LESSON PLAN

Discipline: Elect. Engg.	**Semester:** Fifth (5th)	**Name of the Lab I/C:** Er Debasmita Mohapatra/Er Abadul Sajid Khan
Subject: DE&MP. Lab	**No. of days/week class allotted:** Three (3)	**Semester from Date:** 15.09.22 **to Date:** 22.12.22 **No. of Weeks:** 15
WEEK	**CLASS DAY**	**PRACTICAL EXPERIMENTS**
1st	1st	Verify the truth tables of AND, OR, NOT, NOR, NAND, EX OR &EX NOR GATES.
	2nd	
	3rd	Review Class
2nd	1st	Explain various gates by using universal properties of NAND and NOR gates and verify truth table
	2nd	
	3rd	Review Class
3rd	1st	Implement half adder using logic gates.
	2nd	Implement full adder using logic gates.
	3rd	Review Class
4th	1st	Implement half subtractor using logic gates.
	2nd	Implement full subtractor using logic gates.
	3rd	Review Class
5th	1st	Write a program for 8 bit Addition.
	2nd	
	3rd	Review Class
6th	1st	Write a program for 8-bit Subtraction.
	2nd	

	3rd	Review Class
7th	1st	Study MULTIPLEXER
	2nd	Study DEMULTIPLEXER.
	3rd	Review Class
8th	1st	Study the Operation of Flip Flops.
	2nd	
	3rd	Review Class
9th	1st	Revision
	2nd	
	3rd	
10th	1st	Revision
	2nd	
	3rd	
11th	1st	Revision
	2nd	
	3rd	
12th	1st	Revision
	2nd	
	3rd	
13th	1st	Revision
	2nd	
	3rd	
14th	1st	Revision
	2nd	

	rd 3	
th 15	st 1	Revision
	nd 2	
	rd 3	